ANALOG DEVICES

Quad Precision, High Speed Operational Amplifier

OP467

FEATURES

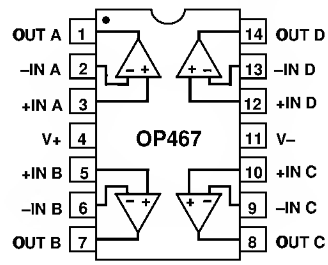
High Slew Rate – 170 V/µs
Wide Bandwidth – 28 MHz
Fast Settling Time – <200 ns to 0.01%
Low Offset Voltage – <500 µV
Unity-Gain Stable
Low Voltage Operation ±5 V to ±15 V
Low Supply Current – <10 mA
Drives Capacitive Loads

APPLICATIONS

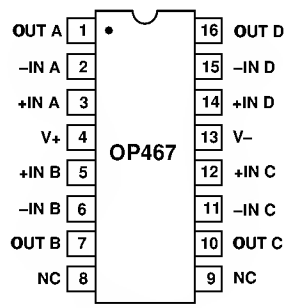
High Speed Image Display Drivers
High Frequency Active Filters
Fast Instrumentation Amplifiers
High Speed Detectors
Integrators
Photo Diode Preamps

PIN CONNECTIONS

14-Lead Ceramic DIP (Y Suffix) and 14-Lead Epoxy DIP (P Suffix)

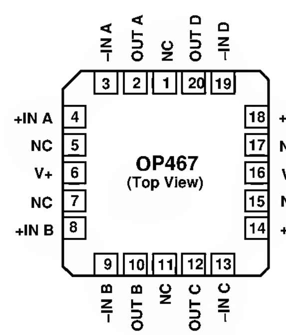


16-Lead SOL (S Suffix)



NC = NO CONNECT

20-Position Chip Carrier (RC Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

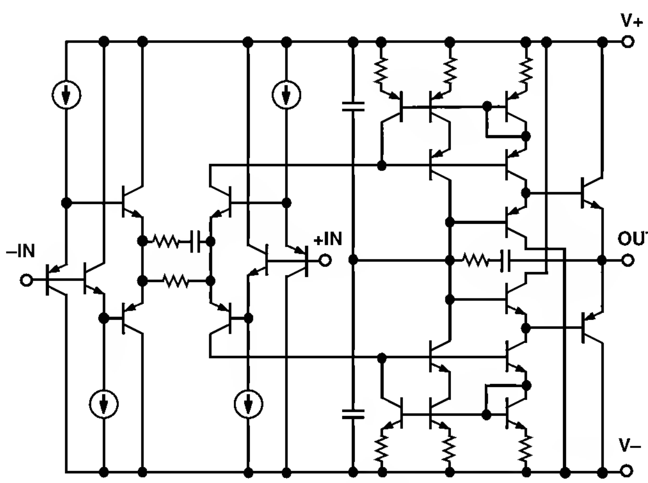
The OP467 is a quad, high speed, precision operational amplifier. It offers the performance of a high speed op amp combined with the advantages of a precision operational amplifier all in a single package. The OP467 is an ideal choice for applications where, traditionally, more than one op amp was used to achieve this level of speed and precision.

The OP467's internal compensation ensures stable unity-gain operation, and it can drive large capacitive loads without oscillation. With a gain bandwidth product of 28 MHz driving a 30 pF load, output slew rate in excess of 170 V/µs, and settling time to 0.01% in less than 200 ns, the OP467 provides excellent dynamic accuracy in high speed data-acquisition systems. The channel-to-channel separation is typically 60 dB at 10 MHz.

The dc performance of OP467 includes less than 0.5 mV of offset, voltage noise density below 6 nV/$\sqrt{Hz}$ and total supply current under 10 mA. Common-mode rejection and power supply rejection ratios are typically 85 dB. PSRR is maintained to better than 40 dB with input frequencies as high as 1 MHz. The low offset and drift plus high speed and low noise, make the OP467 usable in applications such as high speed detectors and instrumentation.

The OP467 is specified for operation from ±5 V to ±15 V over the extended industrial temperature range (–40°C to +85°C) and is available in 14-pin plastic and ceramic DIP, plus SOL-16 and 20-lead LCC surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.



Simplified OP467 Schematic

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	0.5	mV
		$-40°C \le T_A \le +85°C$			1	mV
Input Bias Current	I_B	$V_{CM} = 0$ V		150	600	nA
		$V_{CM} = 0$ V, $-40°C \le T_A \le +85°C$		150	700	nA
Input Offset Current	I_{OS}	$V_{CM} = 0$ V		10	100	nA
		$V_{CM} = 0$ V, $-40°C \le T_A \le +85°C$		10	150	nA
Common-Mode Rejection	CMR	$V_{CM} = \pm 12$V	80	90		dB
	CMR	$V_{CM} = \pm 12$ V, $-40°C \le T_A \le +85°C$	80	88		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2$ kΩ	83	86		dB
		$R_L = 2$ kΩ, $-40°C \le T_A \le +85°C$	77.5			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			0.2		pA/°C
Long Term Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 1			750	μV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	$R_L = 2$ kΩ	±13.0	±13.5		V
		$R_L = 2$ kΩ, $-40°C \le T_A \le +85°C$	±12.9	±13.12		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$\pm 4.5\ V \le V_S = \pm 18$ V	96	120		dB
		$-40°C \le T_A \le +85°C$	86	115		dB
Supply Current	I_{SY}	$V_O = 0$ V		8	10	mA
		$V_O = 0$ V, $-40°C \le T_A \le +85°C$			13	mA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	$A_V = +1$, $C_L = 30$ pF		28		MHz
Slew Rate	SR	$V_{IN} = 10$ V Step, $R_L = 2$ kΩ, $C_L = 30$ pF				
		$A_V = +1$	125	170		V/μs
		$A_V = -1$		350		V/μs
Full-Power Bandwidth	BW_p	$V_{IN} = 10$ V Step		2.7		MHz
Settling Time	t_S	To 0.01%, $V_{IN} = 10$ V Step		200		ns
Phase Margin	θ_0			45		Degrees
Input Capacitance						
Common Mode				2.0		pF
Differential				1.0		pF
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		0.15		μV p-p
Voltage Noise Density	e_N	f = 1 kHz		6		$nV/\sqrt{Hz}$
Current Noise Density	i_N	f = 1 kHz		8		$pA/\sqrt{Hz}$

NOTE
[1]Long Term Offset Voltage Drift is guaranteed by 1000 hrs. Life test performed on three independent wafer lots at +125 °C, with an LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.3	0.5	mV
		$-40°C \le T_A \le +85°C$			1	mV
Input Bias Current	I_B	V_{CM} = 0 V		125	600	nA
		V_{CM} = 0 V, $-40°C \le T_A \le +85°C$		150	700	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		20	100	nA
		V_{CM} = 0 V, $-40°C \le T_A \le +85°C$			150	nA
Common-Mode Rejection	CMR	V_{CM} = ±2.0 V	76	85		dB
	CMR	V_{CM} = ±2.0 V, $-40°C \le T_A \le +85°C$	76	80		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	80	83		dB
		R_L = 2 kΩ, $-40°C \le T_A \le +85°C$	74			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3 5		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			0.2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	±3.0	±3.5		V
		R_L = 2 kΩ, $-40°C \le T_A \le +85°C$	±3.0	±3.20		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±4.5 V ≤ V_S = ±5.5 V	92	107		dB
		$-40°C \le T_A \le +85°C$	83	105		dB
Supply Current	I_{SY}	V_O = 0 V		8	10	mA
		V_O = 0 V, $-40°C \le T_A \le +85°C$			11	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	A_V = +1		22		MHz
Slew Rate	SR	V_{IN} = 5 V Step, R_L = 2 kΩ, C_L = 39 pF				
		A_V = +1		90		V/μs
		A_V = –1		90		V/μs
Full-Power Bandwidth	BW_ρ	V_{IN} = 5 V Step		2.5		MHz
Settling Time	t_S	To 0.01%, V_{IN} = 5 V Step		280		ns
Phase Margin	θ_0			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		0.15		μV p-p
Voltage Noise Density	e_N	f = 1 kHz		7		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		8		pA/√Hz

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		±0.5	mV max
Input Bias Current	I_B	V_{CM} = 0 V	600	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	100	nA max
Input Voltage Range[1]			±12	V min/max
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V	80	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	96	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	83	dB min
Output Voltage Range	V_O	R_L = 2 kΩ	±13.0	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	10	mA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . .±18 V
Input Voltage[2] . . . .±18 V
Differential Input Voltage[2] . . . . ±26 V
Output Short-Circuit Duration . . . . Limited
Storage Temperature Range
  Y, RC Packages . . . .–65°C to +175°C
  P, S Packages . . . .–65°C to +150°C
Operating Temperature Range
  OP467A . . . .–55°C to +125°C
  OP467G . . . .–40°C to +85°C
Junction Temperature Range
  Y, RC Packages . . . .–65°C to +175°C
  P, S Packages . . . .–65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . +300°C

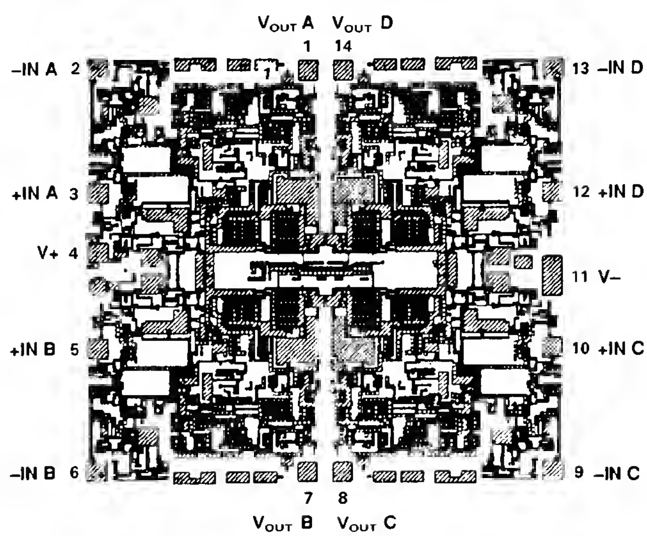
Package Type	θ_{JA}[3]	θ_{JC}	Units
14-Pin Cerdip (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	88	23	°C/W
20-Contact LCC (RC)	78	33	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP467AY/883	–55°C to +125°C	14-Pin Cerdip	Q-14
OP467ARC/883	–55°C to +125°C	20-Contact LCC	E-20A
OP467GP	–40°C to +85°C	14-Pin Plastic DIP	N-14
OP467GS	–40°C to +85°C	16-Pin SOL	R-16
OP467GBC	+25°C	DICE	

DICE CHARACTERISTICS



OP467 Die Size 0.111 × 0.100 inch, 11,100 sq. mils Substrate is Connected to V+, Number of Transistors 165.

Typical Characteristics

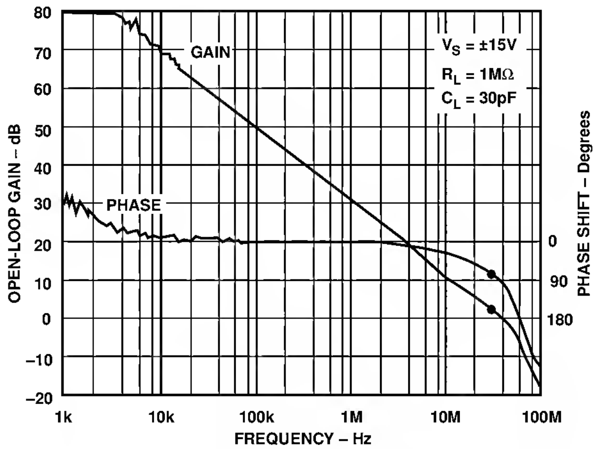


Figure 1. Open-Loop Gain, Phase vs. Frequency

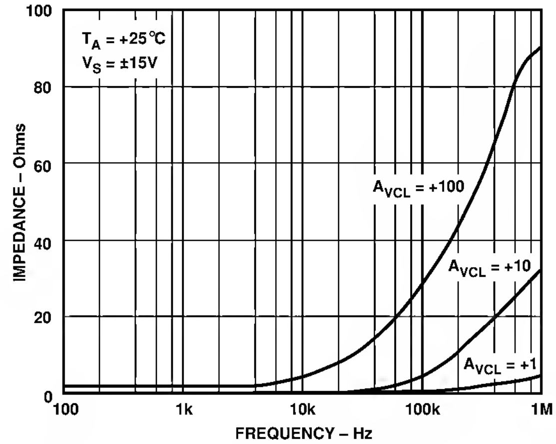


Figure 4. Closed -Loop Output Impedance vs. Frequency

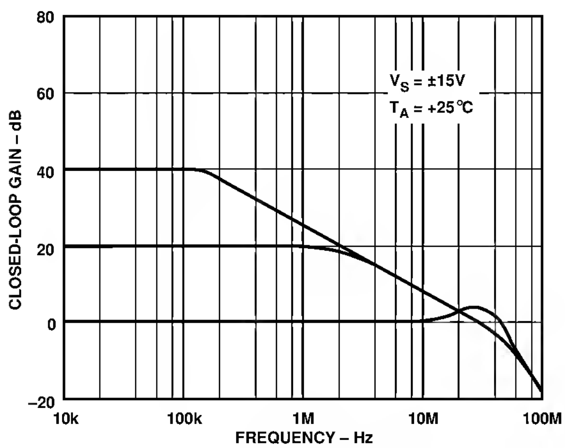


Figure 2. Closed-Loop Gain vs. Frequency

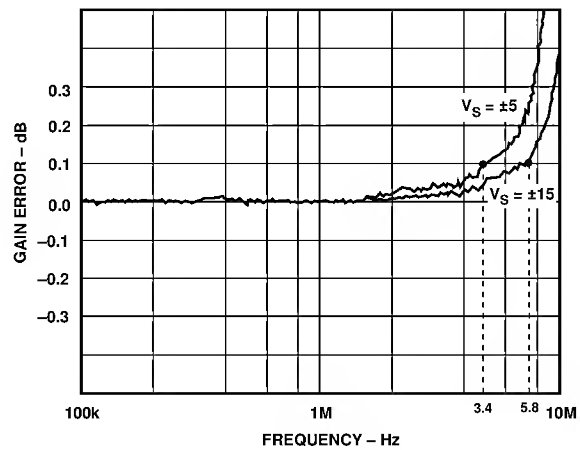


Figure 5. Gain Linearity vs. Frequency

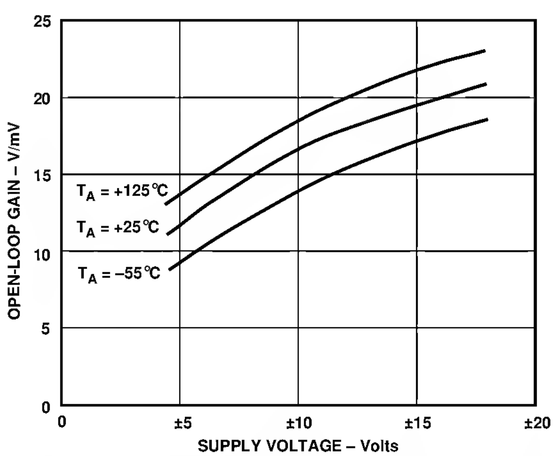


Figure 3. Open-Loop Gain vs. Supply Voltage

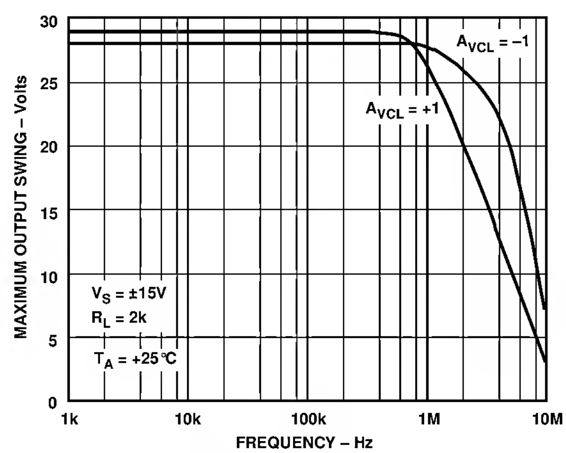


Figure 6. Max V_{OUT} Swing vs. Frequency

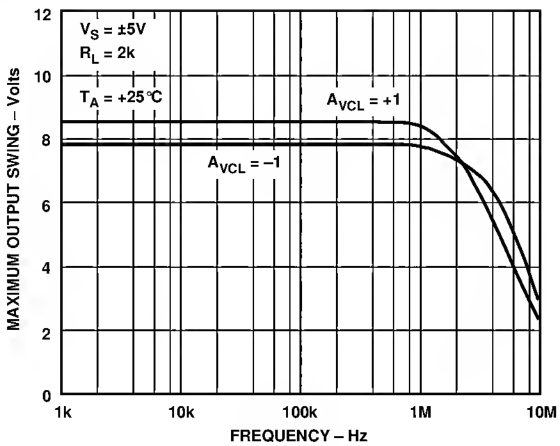


Figure 7. Max V_{OUT} Swing vs. Frequency

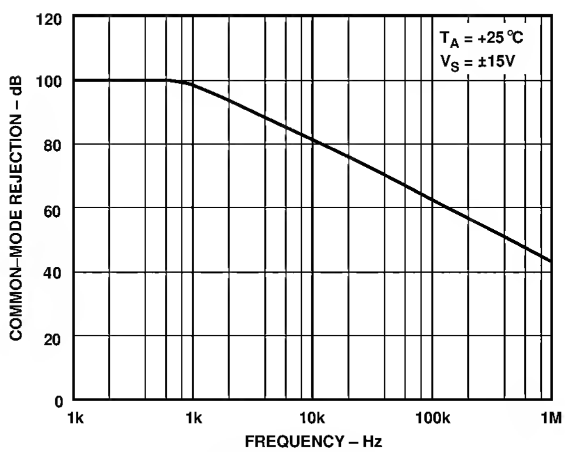


Figure 8. Common-Mode Rejection vs. Frequency

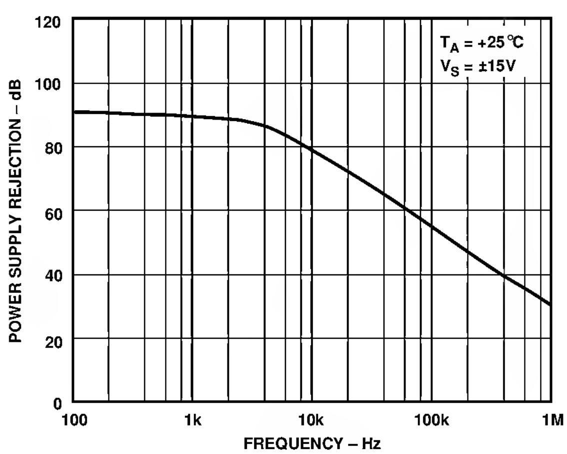


Figure 9. Power-Supply Rejection vs. Frequency

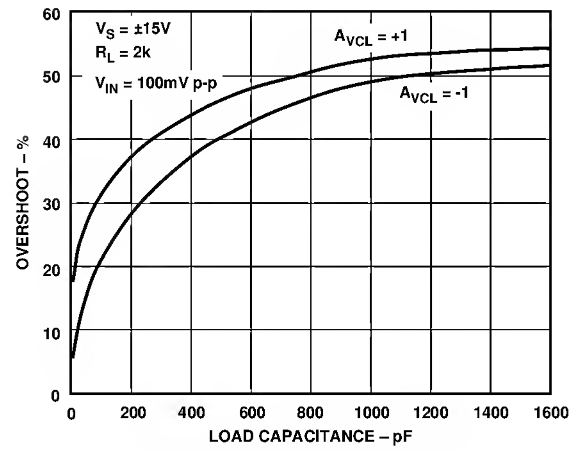


Figure 10. Small Signal Overshoot vs. Load Capacitance

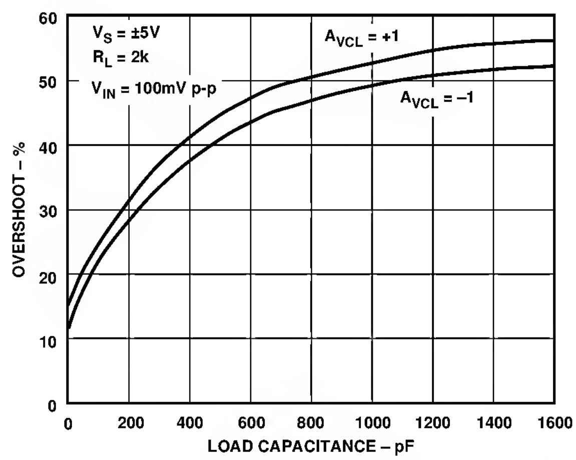


Figure 11. Small Signal Overshoot vs. Load Capacitance

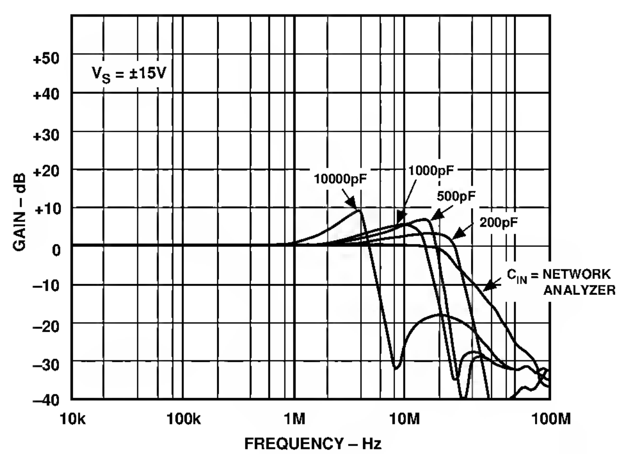


Figure 12. Noninverting Gain vs. Capacitive Loads

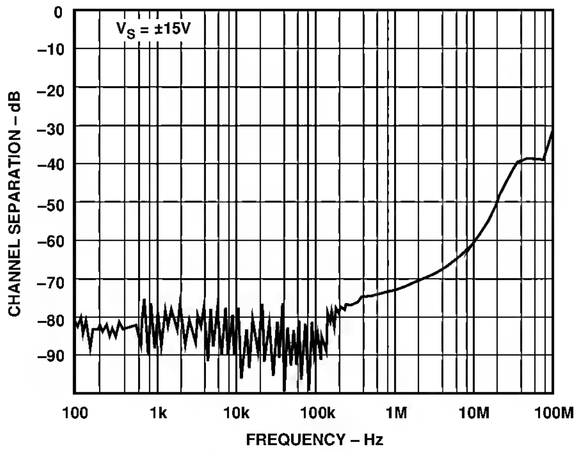


Figure 13. Channel Separation vs. Frequency

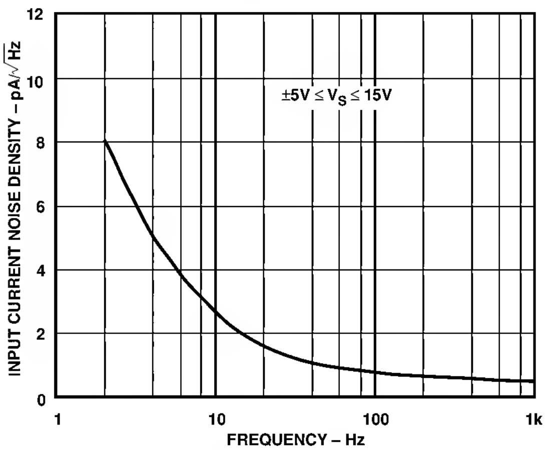


Figure 14. Input Current Noise Density vs. Frequency

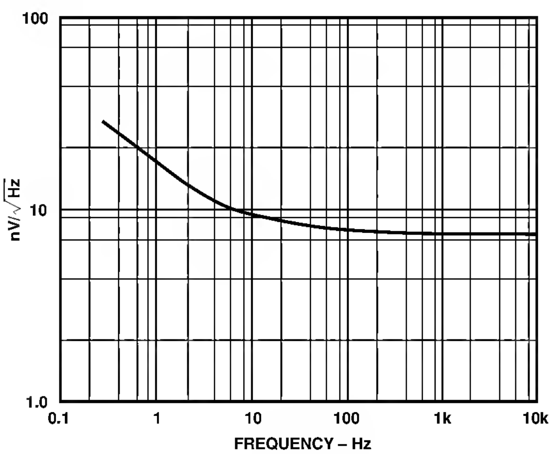


Figure 15. Voltage Noise Density vs. Frequency

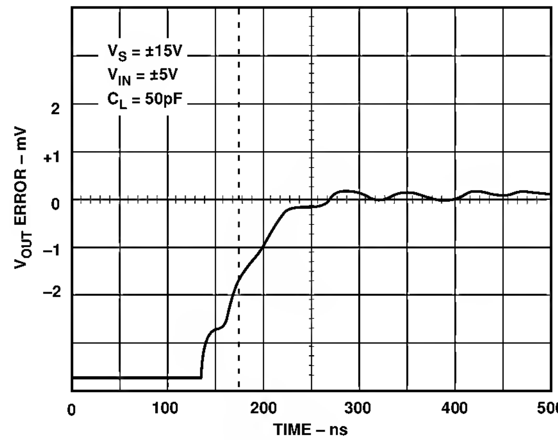


Figure 16. Settling Time, Negative Edge

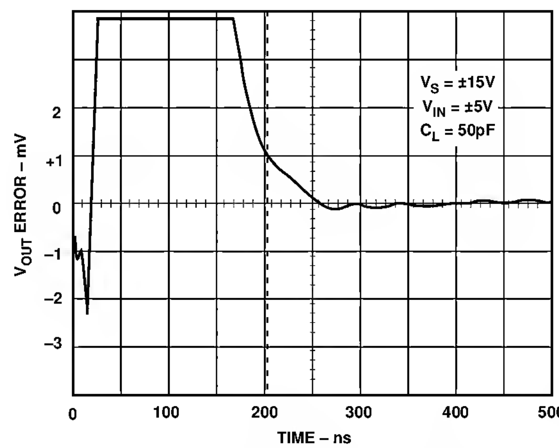


Figure 17. Settling Time, Positive Edge

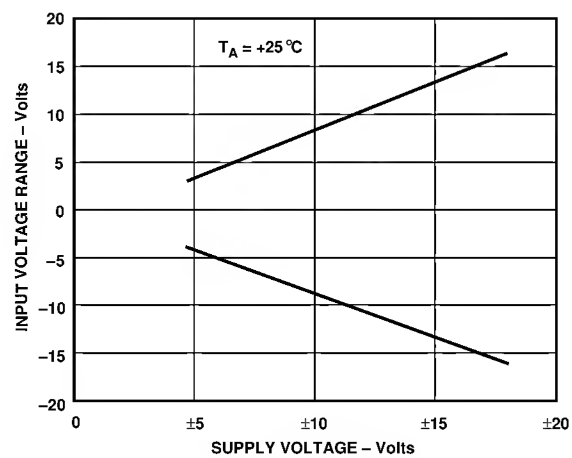


Figure 18. Input Voltage Range vs. Supply Voltage

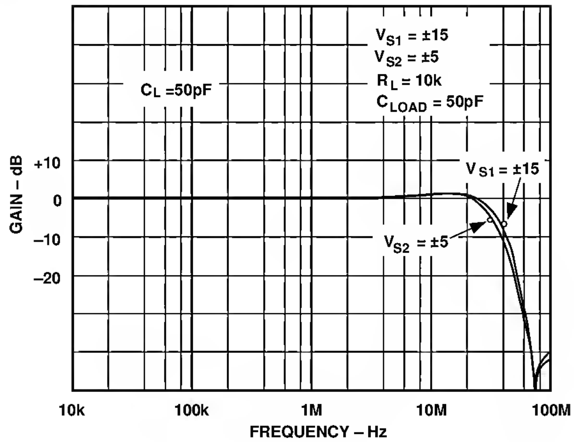


Figure 19. Noninverting Gain vs. Supply Voltage

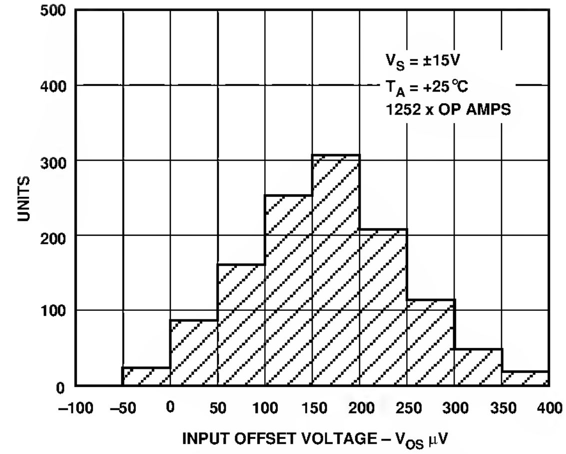


Figure 22. Input Offset Voltage Distribution

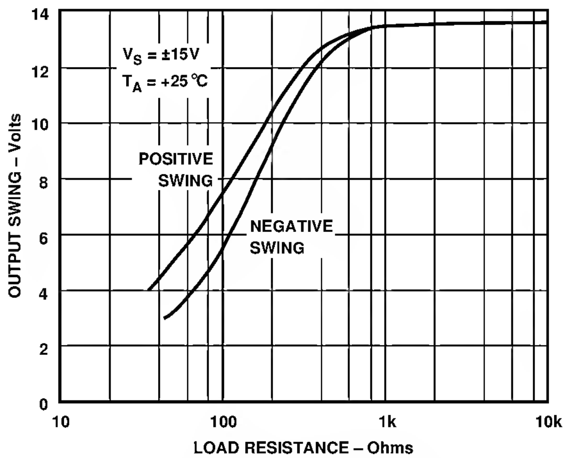


Figure 20. Output Swing vs. Load Resistance

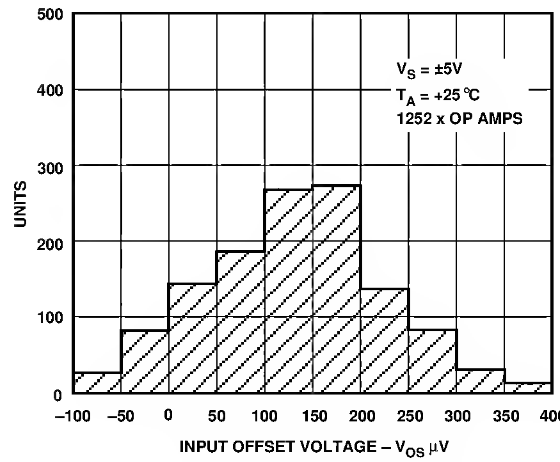


Figure 23. Input Offset Voltage Distribution

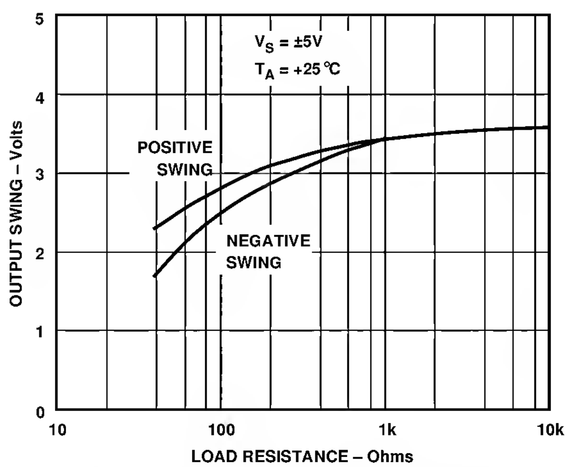


Figure 21. Output Swing vs. Load Resistance

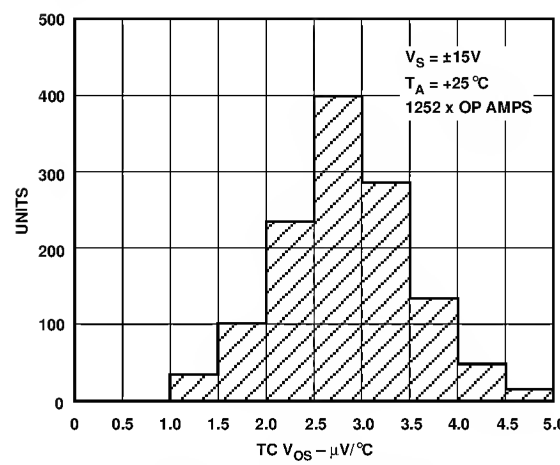


Figure 24. TC V_{OS} Distribution

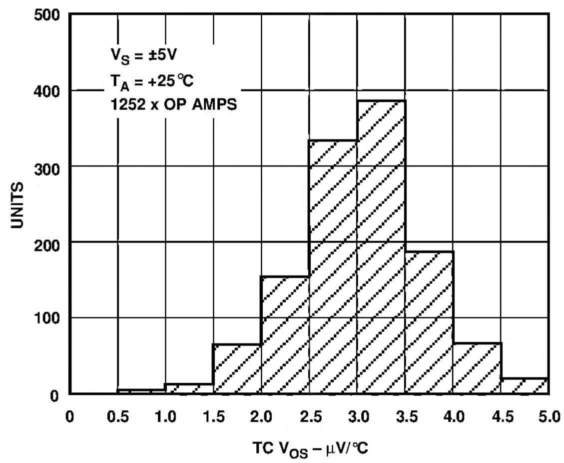


Figure 25. TC V_{OS} Distribution

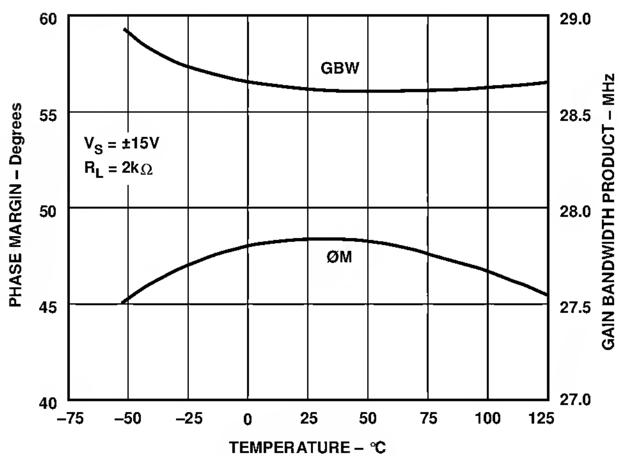


Figure 26. Phase Margin & Gain Bandwidth vs. Temperature

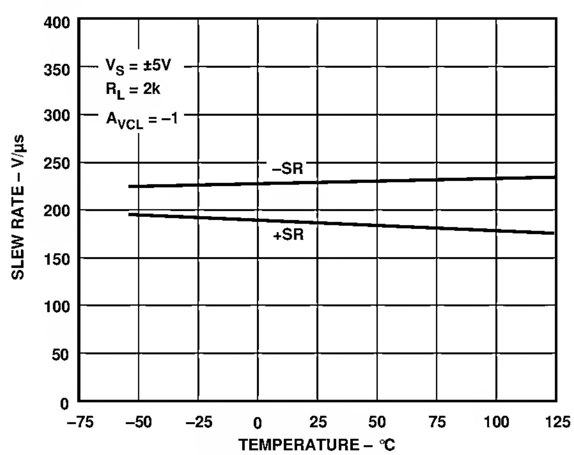


Figure 27. Slew Rate vs. Temperature

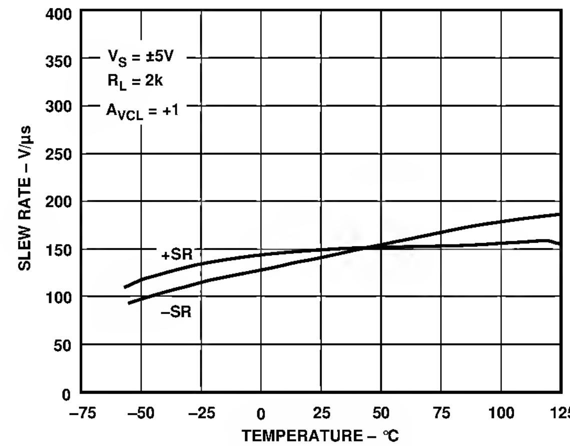


Figure 28. Slew Rate vs. Temperature

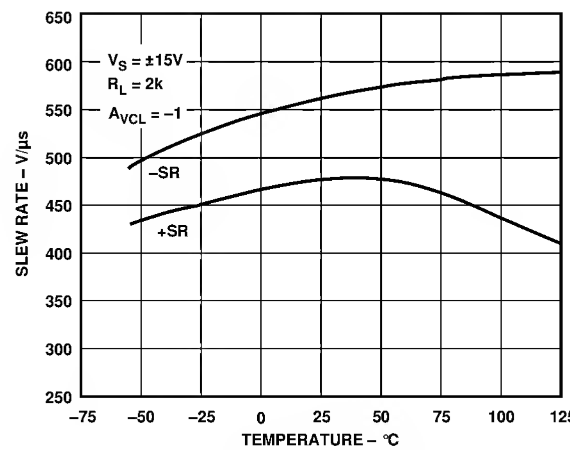


Figure 29. Slew Rate vs. Temperature

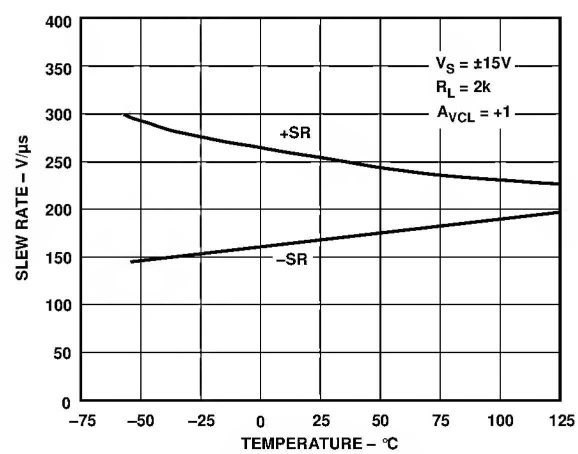


Figure 30. Slew Rate vs. Temperature

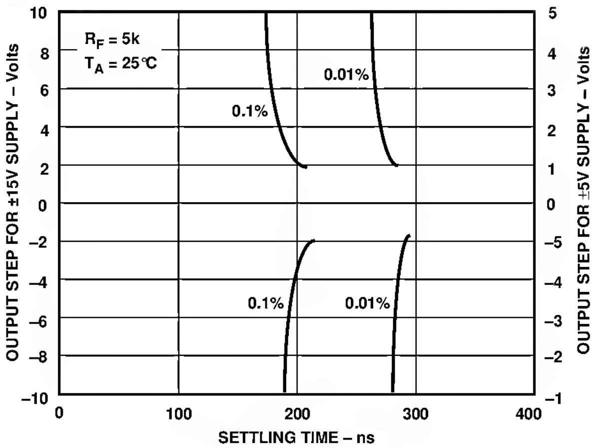


Figure 31. Settling Time vs. Output Step

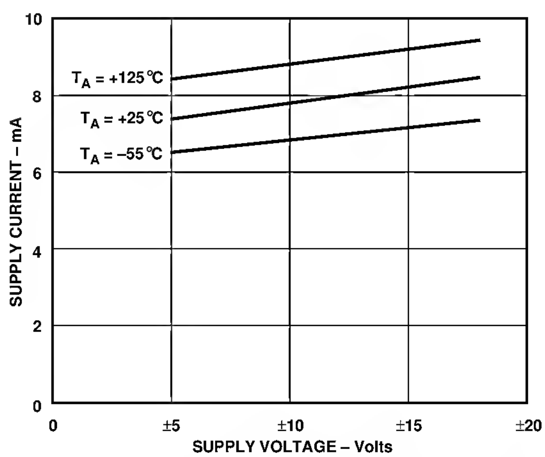


Figure 32. Supply Current vs. Supply Voltage

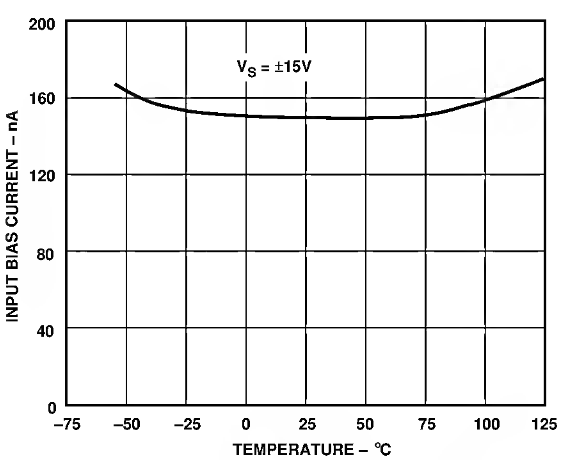


Figure 33. Input Bias Current vs. Temperature

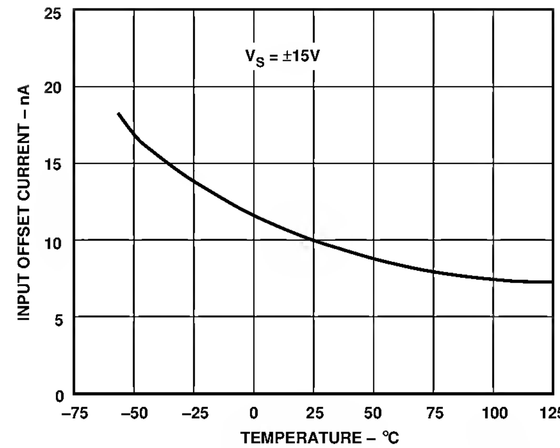


Figure 34. Input Offset Current vs. Temperature

APPLICATIONS INFORMATION

OUTPUT SHORT-CIRCUIT PERFORMANCE

To achieve a wide bandwidth and high slew rate, the OP467 output is *not* short circuit protected. Shorting the output to ground or to the supplies may destroy the device.

For safe operation, the output load current should be limited so that the junction temperature does not exceed the absolute maximum junction temperature.

To calculate the maximum internal power dissipation, following formula can be used:

$$PD = \frac{T_{J\,\max} - T_A}{\theta_{JA}}$$

where T_J and T_A are junction and ambient temperatures respectively, PD is device internal power dissipation, and θ_{JA} is packaged device thermal resistance given in the data sheet.

UNUSED AMPLIFIERS

It is recommended that any unused amplifiers in a quad package be connected as a unity gain follower with a 1 kΩ feedback resistor with noninverting input tied to the ground plain.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Satisfactory performance of a high speed op amp largely depends on a good PC layout. To achieve the best dynamic performance, following high frequency layout technique is recommended.

GROUNDING

A good ground plain is essential to achieve the optimum performance in high speed applications. It can significantly reduce the undesirable effects of ground loops and IR drops by providing a low impedance reference point. Best results are obtained with a multilayer board design with one layer assigned to ground plain. To maintain a continuous and low impedance ground, avoid running any traces on this layer.

POWER SUPPLY CONSIDERATIONS

In high frequency circuits, device lead length introduces an inductance in series with the circuit. This inductance combined with stray capacitance forms a high frequency resonance circuit. Poles generated by these circuits will cause gain peaking and additional phase shift reducing the op amp's phase margin and leading to an unstable operation.

A practical solution to this problem is to reduce the resonance frequency low enough to take advantage of the amplifier's power supply rejection.

This is easily done by placing capacitors across the supply line and the ground plain as close as possible to the device pin. Since capacitors also have internal parasitic components, such as stray inductance, selecting the right capacitor is important. To be effective, they should have low impedance over the frequency range of interest. Tantalum capacitors are an excellent choice for their high capacitance/size ratio, but their ESR (Effective Series Resistance) increases with frequency making them less effective. On the other hand, ceramic chip capacitors have excellent ESR and ESL (Effective Series Inductance) performance at higher frequencies, and because of their small size, they can be placed very close to the device pin, further reducing the stray inductance. Best results are achieved by using a combination of these two capacitors. A 5–10 µF tantalum parallel with a 0.1 µF ceramic chip caps are recommended. If additional isolation from high frequency resonances of the power supply is needed, a ferrite bead should be placed in series with the supply lines between the bypass caps and the power supply. A word of caution, addition of the ferrite bead will introduce a new pole and zero to frequency response of the circuit and could cause unstable operation if it is not selected properly.

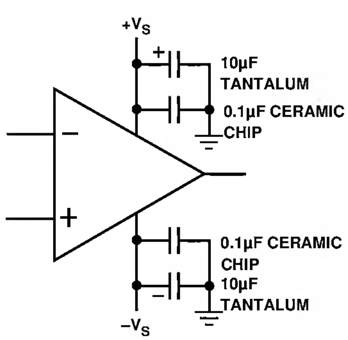


Figure 35. Recommended Power Supply Bypass

SIGNAL CONSIDERATIONS

Input and output traces need special attention to assure a minimum stray capacitance. Input nodes are very sensitive to capacitive reactance, particularly when connected to a high impedance circuit. Stray capacitance can inject undesirable signals from a noisy line into a high impedance input. Protect high impedance input traces by providing guard traces around them. This will also improve the channel separation significantly.

Additionally, any stray capacitance in parallel with the op amp's input capacitance generates a pole in the frequency response of the circuit. The additional phase shift caused by this pole will reduce the circuit's gain margin. If this pole is within the gain range of the op amp, it will cause unstable performance. To reduce these undesirable effects, use the lowest impedance where possible. Lowering the impedance at this node places the poles at a higher frequency, far above the gain range of the amplifier. Stray capacitance on the PC board can be reduced by making the traces narrow and as short as possible. Further reduction can be realized by choosing smaller pad size, increasing the spacing between the traces, and using PC board material with a low dielectric constant insulator (Dielectric Constant of some common insulators: air = 1, Teflon = 2.2, and FR4 = 4.7; with air being an ideal insulator).

Removing segments of the ground plain directly under the input and output pads is recommended.

Outputs of high speed amplifiers are very sensitive to capacitive loads. A capacitive load will introduce a pair of pole and zero to the circuit's frequency response, reducing the phase margin, leading to unstable operation or oscillation.

Generally, it is a good design practice to isolate the amplifier's output from any capacitive load by placing a resistor between the amplifier's output and the rest of the circuits. A series resistor of 10 to 100 ohms is normally sufficient to isolate the output from a capacitive load.

The OP467 is internally compensated to provide stable operation, and is capable of driving large capacitive loads without oscillation.

Sockets are not recommended since they increase the lead inductance/capacitance and reduce the power dissipation of the package by increasing the leads thermal resistance. If sockets must be used, use Teflon* or pin sockets with the shortest leads possible.

PHASE REVERSAL

The OP467 is immune to phase reversal; its inputs can exceed the supply rails by a diode drop without any phase reversal.

*Teflon is a registered trademark of E.I. du Pont Co.

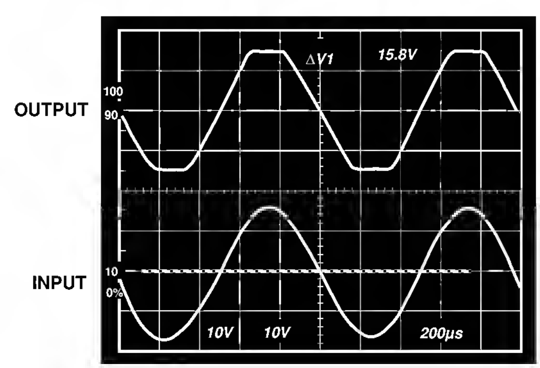


Figure 36. No Phase Reversal ($A_V = +1$)

SATURATION RECOVERY TIME

The OP467 has a fast and symmetrical recovery time from either rail. This feature is very useful in applications such as high speed instrumentation and measurement circuits, where the amplifier is frequently exposed to large signals that overload the amplifier.

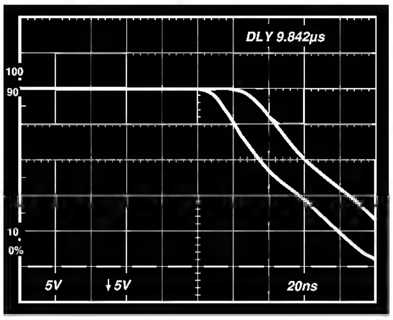


Figure 37. Saturation Recovery Time, Positive Rail

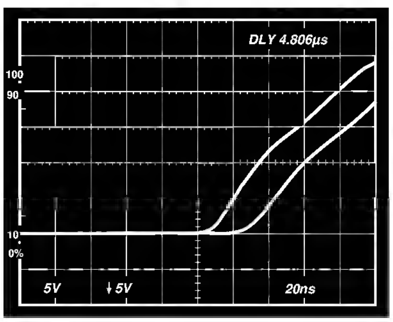


Figure 38. Saturation Recovery Time, Negative Rail

HIGH SPEED INSTRUMENTATION AMPLIFIER

The OP467 performance lends itself to a variety of high speed applications, including high speed precision instrumentation amplifiers. Figure 39 represents a circuit commonly used for data acquisition, CCD imaging, and other high speed application.

Circuit gain is set by R_G. A 2 kΩ resistor will set the circuit gain to 2, for unity gain, remove R_G. For any other gain settings use the following formula:

$$G = 2/R_G \quad \text{Resistor Value is in k}\Omega$$

R_C is used for adjusting the dc common-mode rejection, and C_C is used for ac common-mode rejection adjustments.

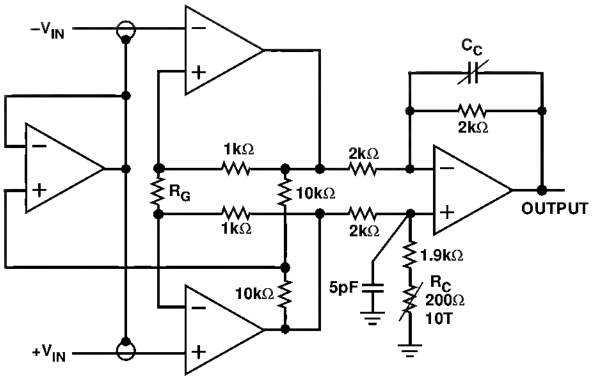


Figure 39. A High Speed Instrumentation Amplifier

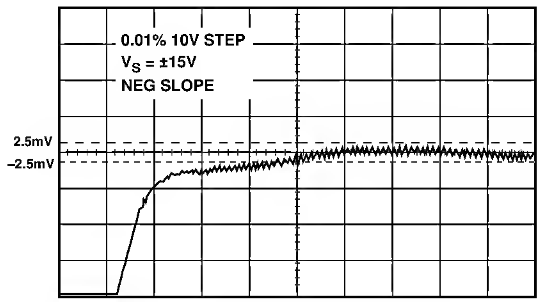


Figure 40. Instrumentation Amplifier Settling Time to 0.01% for a 10 V Step Input (Negative Slope)

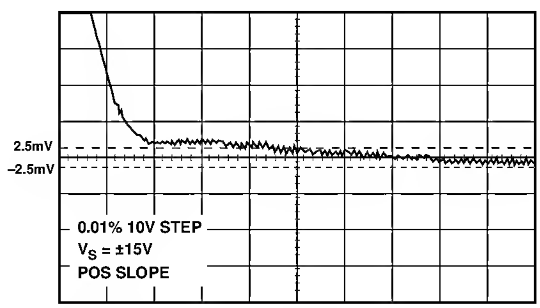


Figure 41. Instrumentation Amplifier Settling Time to 0.01% for a 10 V Step Input (Positive Slope)

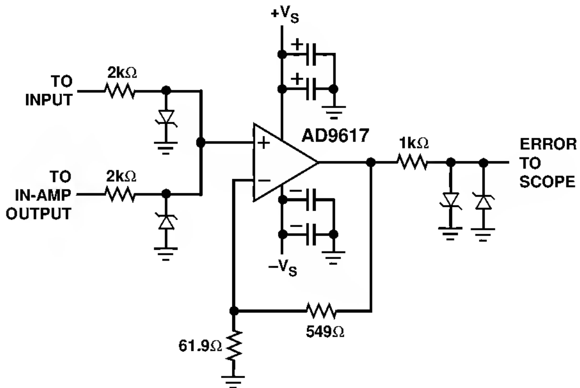


Figure 42. Settling Time Measurement Circuit

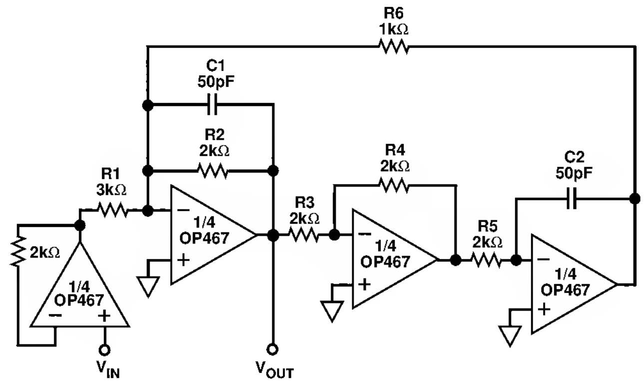


Figure 43. 2 MHz Biquad Filter

2 MHz BIQUAD BANDPASS FILTER

The circuit in Figure 43 is commonly used in medical imaging ultrasound receivers. The 30 MHz bandwidth is sufficient to accurately produce the 2 MHz center frequency, as the measured response shows in Figure 44. When the op amp's bandwidth is too close to the filter's center frequency, the amplifier's internal phase shift causes excess phase shift at 2 MHz, which alters the filter's response. In fact, if the chosen op amp has a bandwidth close to 2 MHz, the combined phase shift of the three op amps will cause the loop to oscillate.

Careful consideration must be given to the layout of this circuit as with any other high speed circuit.

If the phase shift introduced by the layout is large enough, it could alter the circuit performance, or worse, it will oscillate.

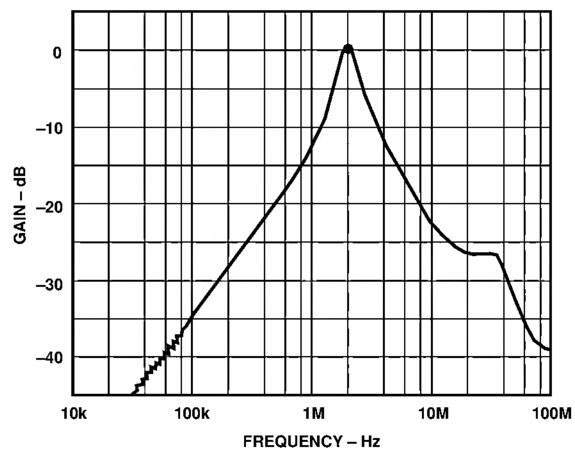


Figure 44. Biquad Filter Response

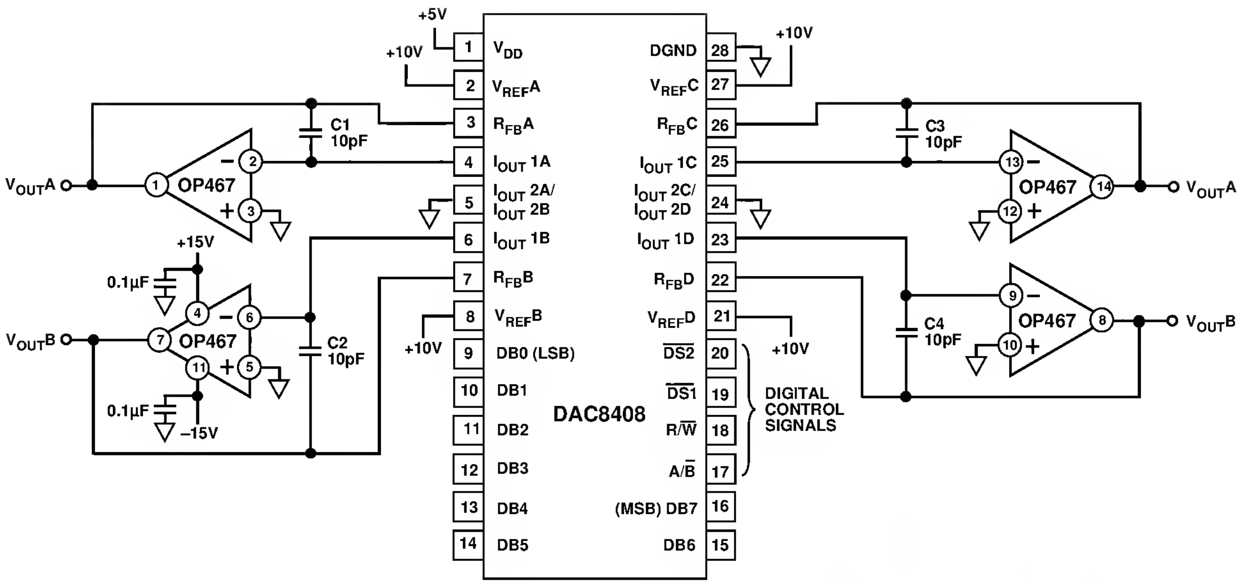


Figure 45. Quad DAC Unipolar Operation

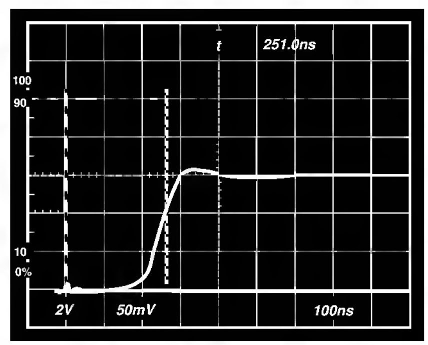


Figure 47. Voltage Output Settling Time

FAST I-TO-V CONVERTER

The fast slew rate and fast settling time of the OP467 are well suited to the fast buffers and I-to-V converters used in variety of applications. The circuit in Figure 45 is a unipolar quad D/A converter consisting of only two ICs. The current output of the DAC8408 is converted to a voltage by the OP467 configured as an I-to-V converter. This circuit is capable of settling to 0.1% within 200 ns. Figures 46 and 47 show the full-scale settling time of the outputs. To obtain reliable circuit performance, keep the traces from the DAC's I_{OUT} to the inverting inputs of the OP467 short to minimize parasitic capacitance.

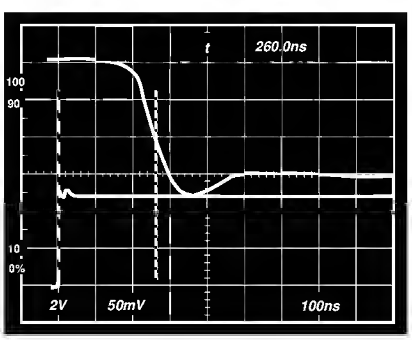


Figure 46. Voltage Output Settling Time

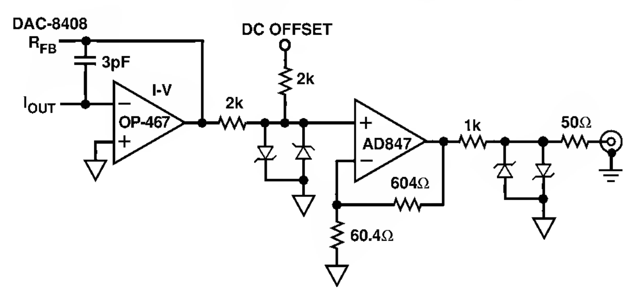


Figure 48. DAC V_{OUT} Settling Time Circuit

OP467 SPICE MACRO-MODEL

```
* Node assignments
                        noninverting input
                        |    inverting input
                        |    |    positive supply
                        |    |    |    negative supply
                        |    |    |    |    output
*                       |    |    |    |    |
. SUBCKT OP467          1    2    99   50   27
*
* INPUT STAGE
*
I1      4    50   10E-3
CIN     1    2    1E-12
IOS     1    2    5E-9
Q1      5    2    8 QN
Q2      6    7    9 QN
R3      99   5    185 . 681
R4      99   6    185 . 681
R5      8    4    180 . 508
R6      9    4    180 . 508
EOS     7    1    POLY (1)  (14,20)  50E-6   1
EREF    98   0    (20,0) 1
*
* GAIN STAGE AND DOMINANT POLE AT 1.5 kHz
*
R7      10   98   3 . 714E6
C2      10   98   28 . 571E-12
G1      98   10   (5,6) 5 . 386E-3
V1      99   11   1 . 6
V2      12   50   1 . 6
D1      10   11   DX
D2      12   10   DX
RC      10   28   1 . 4E3
CC      28   27   12E-12
*
* COMMON-MODE STAGE WITH ZERO AT 1.26 kHz
*
ECM     13   98   POLY (2)   (1,20)    (2,20) 0 0 . 5 0 . 5
R8      13   14   1E6
R9      14   98   25 . 119
C3      13   14   126 . 721E-12
*
* POLE AT 400E6
*
R10     15   98   1E6
C4      15   98   0 . 398E-15
G2      98   15   (10,20) 1E-6
*
* OUTPUT STAGE
*
ISY     99   50   -8 . 183E-3
RMP1    99   20   96 . 429E3
RMP2    20   50   96 . 429E3
RO1     99   26   200
RO2     26   50   200
L1      26   27   1E-7
GO1     26   99   (99,15) 5E-3
GO2     50   26   (15,50) 5E-3
G4      23   50   (15,26) 5E-3
G5      24   50   (26,15) 5E-3
V3      21   26   50
V4      26   22   50
D3      15   21   DX
D4      22   15   DX
D5      99   23   DX
D6      99   24   DX
D7      50   23   DY
D8      50   24   DY
*
* MODELS USED
*
. MODEL QN NPN (BF=33.333E3)
. MODEL DX D
. MODEL DY D (BV=50)
. ENDS OP467
```

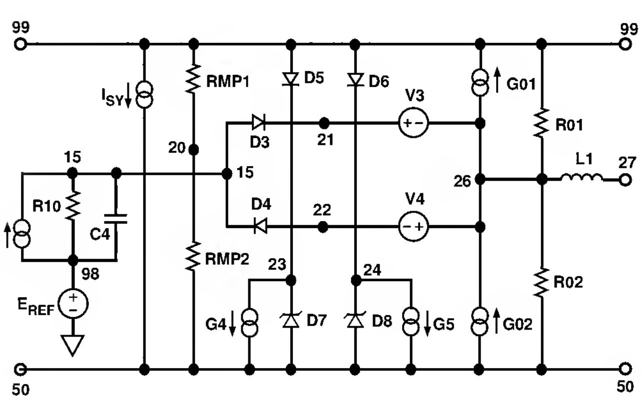


Figure 49. Spice Macro-Model Output Stage

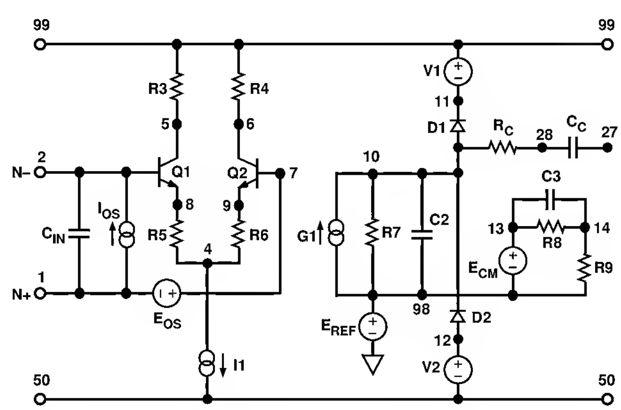
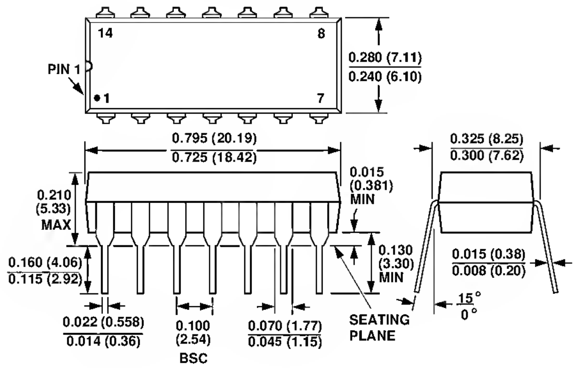


Figure 50. Spice Macro-Model Input and Gain Stage

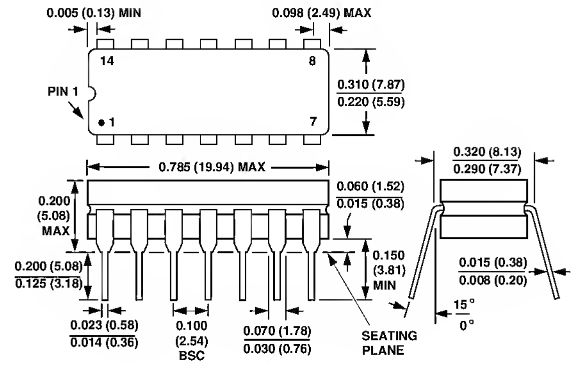
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

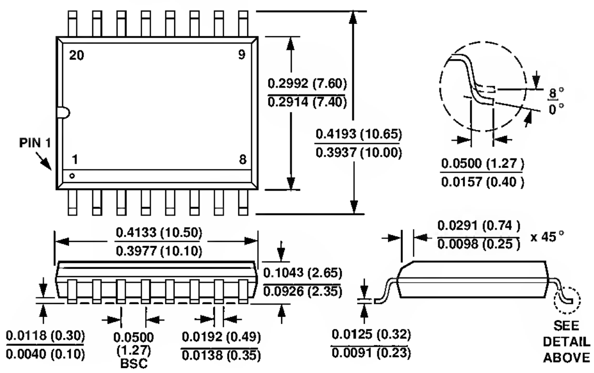
14-Lead Plastic DIP (P Suffix)



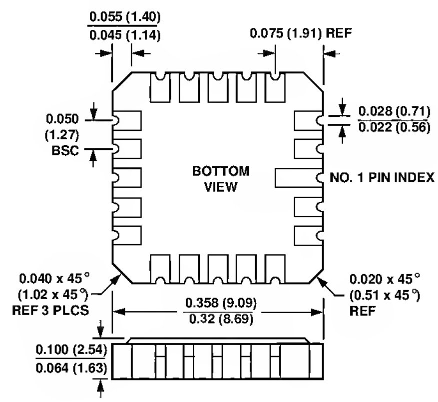
14-Lead Cerdip (Y Suffix)



16-Lead Wide-Body SOL (S Suffix)



20-Terminal Leadless Ceramic Chip Carrier (RC Suffix)



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